CLAIMS

1. A branch predictor for a multi-processing computer comprising:

a history register for storing a branch history of previous sequential branch instructions;

a hash logic for creating an index from a combination of process references corresponding to a current branch instruction, an address of the current branch instruction, and the branch history;

a branch prediction table for storing branch prediction reference data, and for outputting branch prediction reference data corresponding to the index created by the hash logic;

an address selection circuit for selecting one of a target address known from the current branch instruction and a next instruction of the current branch instruction to generate a branch prediction address, in response to the branch prediction reference data output from the branch prediction table; and

a branch prediction result tester for updating the branch history stored in the history register and the branch prediction reference data stored in the branch prediction table, in response to a real branch address and the branch prediction address according to an execution result of the current branch instruction.

2. The branch predictor of Claim 1, wherein the branch prediction table comprises a plurality of up/down saturating counters selected by the index created by the hash logic.

3. The branch predictor of Claim 1, wherein the history register comprises a shift register.

4. The branch predictor of Claim 1, wherein the hash logic creates the index by performing an exclusive-OR operation to the process ID corresponding to the current branch instruction, the address of the current branch instruction, and the branch history.

5. The branch predictor of Claim 1, wherein the branch prediction result tester includes a comparator for determining whether a real branch address according to an execution result of the current branch instruction matches with the branch prediction address, and creating a control signal corresponding to the result.

6. The branch predictor of Claim 5, wherein the comparator generates a control signal of logic “1” if the real branch address matches with the branch prediction address, and generates a control signal of logic “0” if the real branch address does not match.

7. The branch predictor of Claim 6, wherein the address selection circuit changes and outputs the real branch address to the corrected branch address when the control signal is logic “0”.

8. The branch predictor of Claim 6, wherein the counter increments when the control signal is logic “1”, and counts decrements when the control signal is logic “0”.

9. The branch predictor of Claim 6, wherein the shift register shifts the branch prediction result in a first direction by inserting the control signal.

10. A prediction method of a branch address of a conditional branch instruction with reference to a branch prediction table for storing branch prediction reference data, the method comprising the steps of:

creating an index to access the branch prediction table from a combination of a process ID corresponding to the conditional branch instruction, an address of the conditional branch instruction, and previous sequential branch instructions;

reading branch prediction reference data from the branch prediction table in response to the index;

selectively outputting one of a target address known from the conditional branch instruction and a next address of the conditional branch instruction in response to the branch prediction reference data; and

updating the branch history and the stored branch prediction reference data in the branch prediction table in response to a real branch address according to an execution result of the conditional branch instruction.

11. The method of Claim 10 further comprising the steps of:

determining whether the real branch address matches with the branch prediction address; and

changing and outputting the corrected branch address to the branch address if the real branch address does not match therewith.